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RESEARCH ARTICLE

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# Integrated potentiostat for detection of Chagas disease

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**Summary**

The design of a low-power-integrated potentiostat that measures electric current intended for a Chagas disease detection application is presented. This circuit can generate and measure currents from 1 to 10 μA with a relative error under 5%. The remaining part of the circuit consumes only 1.5 μA. The circuit was designed using the 0.6 μm XC06 technology from the X-FAB, with a total silicon area of 0.24 $mm^2$ (without pads).

**KEYWORDS**

Chagas disease, integrated circuits, low power, potentiostat

## 1 | INTRODUCTION

Chagas disease is an infection caused by a parasite (*Trypanosoma cruzi*), which nowadays affects more than 10-million people from Latin America (five times more than HIV). A conclusive diagnosis of Chagas disease consists of using a microscope to find the parasite in blood samples. This procedure requires highly qualified personnel, which results in high costs and a need for well-equipped installations, which are not always available in impoverished areas in rural South America.[1,2] These drawbacks could be overcome by a simple and robust tool, which allows in situ diagnosis that could be operated by local health workers, as is proposed by the project point-of-care print (PoC-print).[3]

Over the last few years, *lab-on-chip* platforms for Chagas disease diagnosis have been reported,[4] which display excellent results when compared with traditional methods, adding portability and shorter incubation times.[3,5] However, due to the traditional silicon-based technologies, the cost of these platforms is too high, hindering its market application.

The aim of this project is to develop an application-specific integrated circuit (ASIC) potentiostat to measure electric current to detect the presence of Chagas disease for integration with the PoC-Print target device. This work continues the one in Martín et al[4] but reduces power consumption, welding spots, and number of components and reduces cost through the integration process. With the reduced power and cost, a disposable testing device, powered by near-field communication (NFC), can be implemented. This integrated circuit is a potentiostat, which is composed by an operational transconductance amplifier (OTA) and an output stage, a current-controlled oscillator in order to measure the output current of the potensiostat, and an eight-channel analog multiplexer for multiple electrode capabilities were included. The full ASIC is shown in Figure 1. Both designs are based on an existing work,[4] optimizing to reduce current consumption while keeping a small measurement error (5% maximum error). During the design, transistors were modelled using a single equation model for all modes of operation, the advanced compact metal-oxide-semiconductor field-effect transistor (MOSFET) (ACM),[6] due to its simplicity for hand calculations, while transistor thermal and flicker noise were modelled using the studies of Pierce[7] and Arnaud and Galup-Montoro,[8,9] respectively.

In the complete PoC disposable system, circuit power will be supplied by a market NFC chip, which will be part of PoC-print-printed circuit board (PCB), together with a precise voltage reference. Silicon area of the ASIC is bounded by 2.5 $mm^2$, pads included. The complete system and a block diagram of the ASIC can be found in Figures 1 and 2, respectively.

  

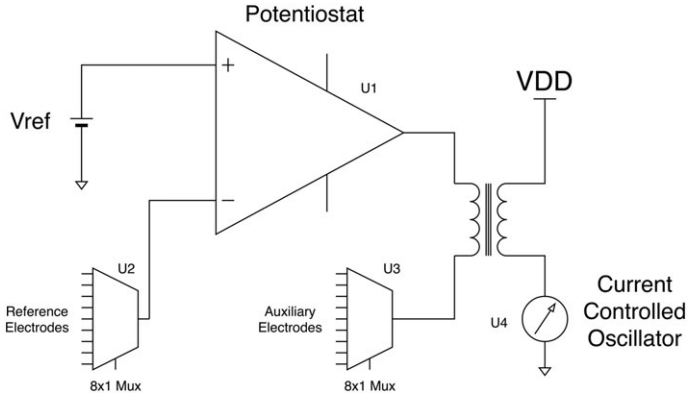


**FIGURE 1** Block diagram of the designed application-specific integrated circuit (ASIC)

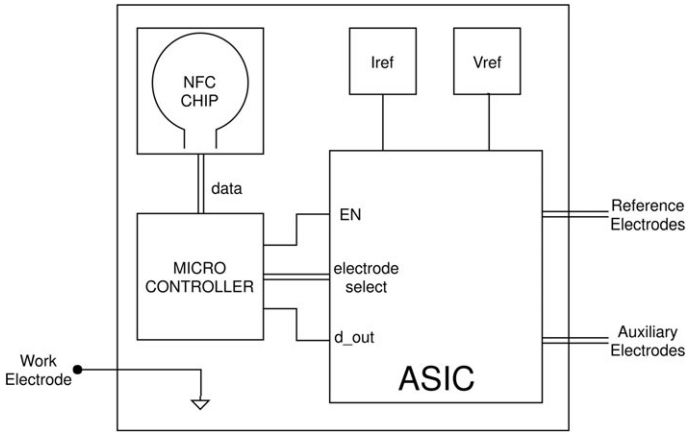


**FIGURE 2** Block diagram of the point-of-care (PoC)-print-printed circuit board (PCB) in which the application-specific integrated circuit (ASIC) is designed to operate

Electrochemical detection is achieved through a potentiostat, which is an electronic device that controls a three-electrode cell submerged in a fluid sample. The potentiostat keeps the reference electrode at a fixed voltage from the work electrode, by means of adjusting the current in the auxiliary electrode, as is shown in Figure 3.

Electrodes can be represented as wires, and the fluid sample and the electrode-fluid interphase can be represented as electrical resistances between the electrodes, as shown in Figure 4. The potentiostat operates in an equivalent

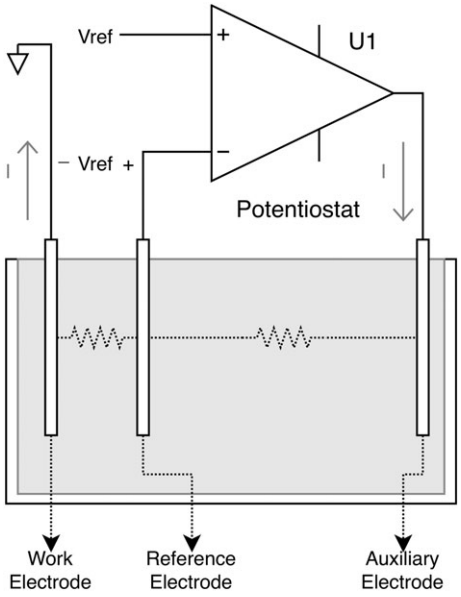


**FIGURE 3** Diagram of the potentiostat submerged in a fluid sample

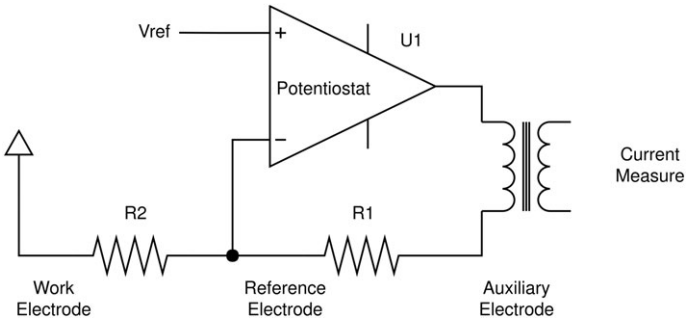


**FIGURE 4** Electrical schematic of the potentiostat as an operational amplifier in noninverting configuration

manner to an operational amplifier in noninverting configuration, and the relevant output measure is the current injected through the auxiliary electrode. Since the reference electrode draws no current, this current is proportional to the equivalent electrical resistance of the fluid between the reference and work electrodes. The output current may vary between 1, when the parasite is not present in the blood sample, and 10 μA when the blood sample contains the parasite.[5]

## 2 | CIRCUIT DESCRIPTION

### 2.1 | Potentiostat

The potentiostat is composed by an OTA and an output stage, presented in Figures 5 and 6.

The OTA configuration shown in Figure 5 was chosen because it provides a large output voltage swing on the node $I_{\text{out}}$,[10] which allows for a larger operation area of the potentiostat shown in Figure 6.

For the output stage, an N-type metal-oxide-semiconductor (NMOS) transistor and a cascode current mirror with a 100 to one relation were used. The copy is performed so that the measurement does not affect the potentiostat performance, and current scaling is done to reduce the circuit's total current consumption, while still maintaining a value high enough to be measured without issues. Cascode topology is implemented to achieve the maximum accuracy, since this current is the most critical measure in the circuit.

From circuits shown in Figures 4 and 6, a transfer function can be obtained from input $V_{\text{ref}}$ to output current, as shown in Equation 1.

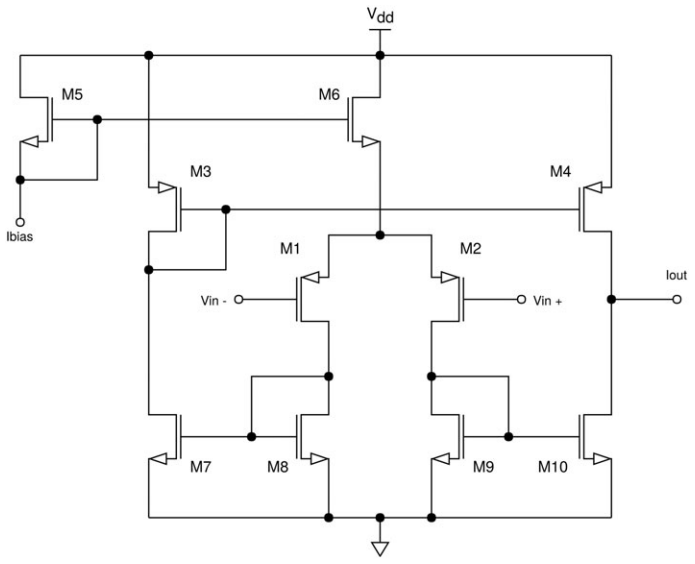


**FIGURE 5** Transistor level schematic of the operational transconductance amplifier (OTA) in the potentiostat. All P-type metal-oxide-semiconductor (PMOS) transistors' bulks are connected to $V_{DD}$, apart from M1 and M2, which have their bulks connected to their source. All N-type metal-oxide-semiconductor (NMOS) transistors' bulks are connected to $G_{nd}$

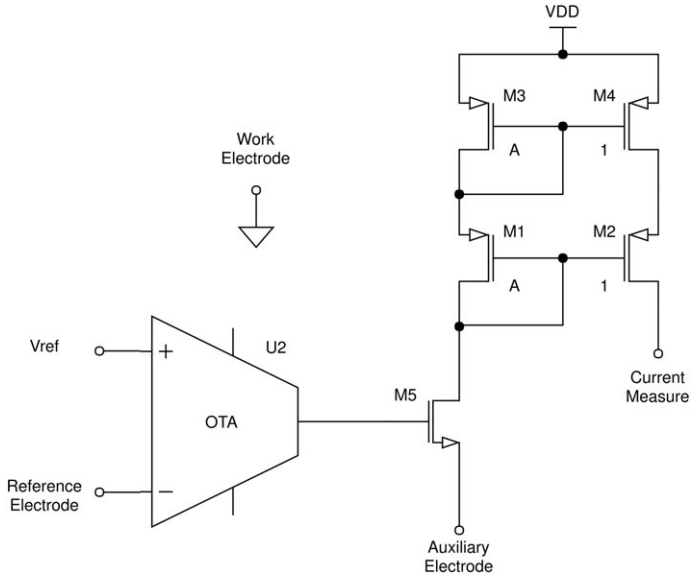


**FIGURE 6** Schematic of the potentiostat. All P-type metal-oxide-semiconductor (PMOS) transistors have their bulk connected to $V_{DD}$, and all N-type metal-oxide-semiconductor (NMOS) transistors have their bulk connected to $G_{nd}$

$$H(j\omega) = \frac{\frac{1}{AR_2}}{\left(1 + j\frac{\omega}{\frac{g_{M5}g_M R_2}{C}}\right)}, \tag{1}$$

where $A$ is the scale factor in the output current mirror, $R_2$ is the equivalent electrical resistance between reference and work electrodes, $g_{M5}$ is the transconductance of transistor M5 from Figure 6, $g_M$ is the transconductance of the OTA, and $C$ is the gate capacitance of transistor M5.

The ACM model shown in Cunha et al[6] and the classic thermal and flicker transistor noise models in Pierce, Arnaud and Galup-Montoro, and Miguez[7-9] were used to calculate noise and dimensions for the transistors. With those models in mind, thermal noise for the OTA was calculated as is shown in Equation 2.

$$S_{\text{VinOTA}} = 2\,S_{\text{VinM1}}\left[1 + \frac{\left(\frac{g_{M8}}{I_{D8}}\right)}{\left(\frac{g_{M1}}{I_{D1}}\right)} + \frac{\left(\frac{g_{M7}}{I_{D7}}\right)}{\left(\frac{g_{M1}}{I_{D1}}\right)} + \frac{\left(\frac{g_{M3}}{I_{D3}}\right)}{\left(\frac{g_{M1}}{I_{D1}}\right)}\right], \tag{2}$$

where $g_{mi}$ *and* $I_{Di}$ are the transconductance and drain-source current of the $i_{th}$ transistors, and $S_{\text{VinM1}} = \frac{\gamma n K_B T}{I_{D1}} \frac{1}{\frac{g_{M1}}{I_{D1}}}$, where $K_B$ is the Boltzmann constant, $T$ is the absolute temperature, $n \approx 1$ is the slope factor, and $\gamma = 2\,o\,\frac{8}{3}$ for strong or weak inversion, respectively.

From Equation 2, it can be deduced that to minimize thermal noise on the OTA, transistors M1 and M2 must be in weak inversion to maximize the $\frac{g_M}{I_D}$ ratio, while the rest should be on strong or moderate inversion to minimize the ratio. Table 1 presents transistors' sizes, polarization currents, and transconductance values for the OTA transistors.

To calculate the thermal noise for the transistors of the potentiostat, the small signal circuit for noise analysis is shown in Figure 7.

For the rest of the potentiostat transistors, feedback by the R1 and R2 resistors causes the current thermal noise generated by each transistor to be applied directly onto the load resistors, and consequently, a voltage noise signal is produced on the working electrode of value $R_1$. $i_{noise}$, which is transferred directly to the input $V_{ref}$, canceling this effect.

As shown by previous studies,[11] in a cascode current mirror, the only transistors that contribute to the current mirror noise are those that have their source directly connected to $G_{nd}$ for NMOS and $V_{dd}$ for P-type metal-oxide-

**TABLE 1** Operational transconductance amplifier (OTA) transistor sizes and transconductances

| Transistor Name (See Figure 5) | W/L (μm) | Transconductance (nS) |
|---|---|---|
| M1, M2 | 111/15 | 823 |
| M3, M4 | 3/12 | 449 |
| M5, M6 | 6/12 | 899 |
| M7, M8, M9, M10 | 6/12 | 440 |

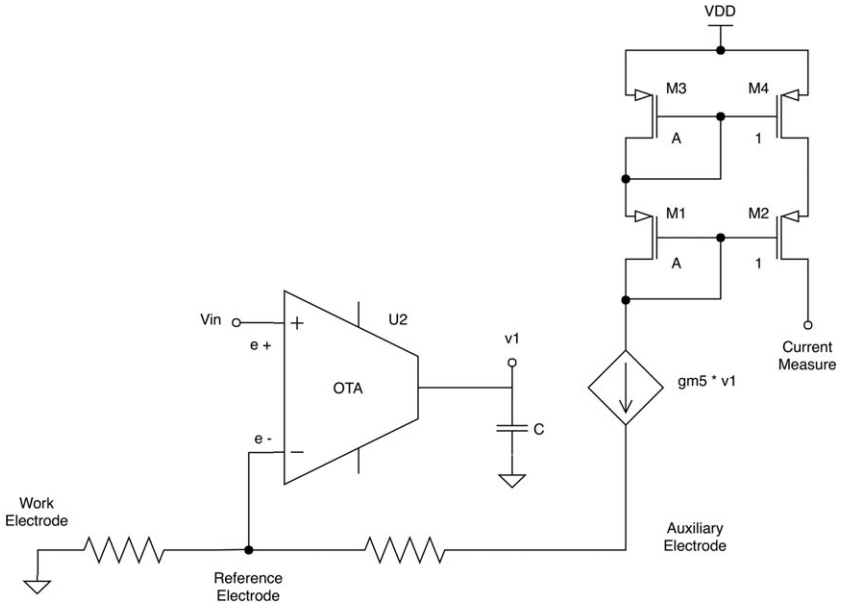


**FIGURE 7** Potentiostat small signal model

semiconductor (PMOS). Therefore, transistors M2 and M4 do not add noise to the circuit. Noise generated in parallel with the drain-source current of transistor M3 is injected directly into the output, so its effect at the input can be obtained simply by dividing it by the square of the transfer module shown in Equation 1.

The noise generated in parallel with the drain-source current of transistor M1 can be carried out by multiplying by $A^2$, the square of the scaling relationship of the M1 to M4 current mirror. Next, divide between the transfer module squared to determine the effect back at the input. The same process is done for transistor M5.

Finally, Equation 3 is obtained as follows:

$$S_{V_{in}} = S_{V_{in}\mathrm{OTA}} + \frac{\gamma\, n\, K_B\, T\, I_{\mathrm{D3}}}{|H(j\omega)|^2}\left[\frac{g_{\mathrm{M3}}}{I_{\mathrm{D3}}} + \frac{1}{A}\left(\frac{g_{\mathrm{M5}}}{I_{\mathrm{D5}}} + \frac{g_{\mathrm{M1}}}{I_{\mathrm{D1}}}\right)\right], \tag{3}$$

where $S_{V_{in}\mathrm{OTA}}$ is the one shown in Equation 2, $g_{mi}$ and $I_D$ are the transconductance and drain-source current of transistor $i$, $A$ is the scaling relationship of the M1 to M4 current mirror, $H(j\omega)$ is the one shown in Equation 1, and all other constants are the same as the ones for Equation 2.

From Equation 3, it follows that all transistors of the potentiostat outside the OTA must be working in moderate or strong inversion to minimize noise at the input. Since the measure of interest of the potentiostat is direct current and it will operate at low frequencies, the pole of the transfer of the potentiostat can be neglected (with the proposed values, a pole is in the order of megahertz).

Since $A$ is greater than 1, it can be seen from Equation 3 that the most critical transistor for the input noise in the potentiostat is M3. This is consistent with what we expected since its noise is applied directly to the output.

To study flicker noise, the same calculations were performed but with the flicker noise power spectral density (PSD) model shown in Pierce, Arnaud and Galup-Montoro, and Miguez.[7-9] Under these conditions, the following equations are obtained:

$$S_{v_{in}\mathrm{M1_{OTA}}} = \frac{q^2 N_{ot}}{WLC'_{ox}} \cdot \frac{1}{f}, \tag{4}$$

$$S_{Vin_{\mathrm{OTA}}} = 2\, S_{V_{in}M1_{\mathrm{OTA}}} \left[ 1 + \frac{\left(\frac{g_{\mathrm{M8}}}{I_{\mathrm{D8}}}\right)^2}{\left(\frac{g_{\mathrm{M1}}}{I_{\mathrm{D1}}}\right)^2} + \frac{\left(\frac{g_{\mathrm{M7}}}{I_{\mathrm{D7}}}\right)^2}{\left(\frac{g_{\mathrm{M1}}}{I_{\mathrm{D1}}}\right)^2} + \frac{\left(\frac{g_{\mathrm{M3}}}{I_{\mathrm{D3}}}\right)^2}{\left(\frac{g_{\mathrm{M1}}}{I_{\mathrm{D1}}}\right)^2} \right], \tag{5}$$

$$S_{V_{in}} = S_{V_{in}\mathrm{OTA}} + \frac{q^2 N_{ot} I_{\mathrm{D3}}^2}{WLC'_{ox} f\, |H(j\omega)|^2} \left[ \left(\frac{g_{\mathrm{M3}}}{I_{\mathrm{D3}}}\right)^2 + \left(\frac{g_{\mathrm{M5}}}{I_{\mathrm{D5}}}\right)^2 + \left(\frac{g_{\mathrm{M1}}}{I_{\mathrm{D1}}}\right)^2 \right], \tag{6}$$

where $q$ is the charge of the electron, $W$, $L$, and $C'_{ox}$ are the length, width, and capacity per unit area of the transistor, respectively, and $N_{ot}$ is the effective number of traps.[12]

As can be seen from Equations 4 to 6 because of the similarity of the PSDs, the transistors should operate at the same inversion level as determined by the thermal noise analysis. The only difference between flicker and thermal noise is that none of the transistors of the output stage of the potentiostat are multiplied by 1/A, so they all have equal weight in the contribution of noise. To minimize flicker noise, the transistor sizes are adjusted (increased) until an acceptable noise level. Table 2 presents transistors sizes, polarization currents, and transconductance values for the potentiostat transistors.

Due to imperfections in the manufacturing process, no transistor is identical to another, even if in theory they are designed that way. It can be experimentally demonstrated that $V_{th}$ and $\beta$ follow a normal distribution, where the mean for $V_{th}$ and $\beta$ and their deviations $\sigma_{V_{th}}$ and $\sigma_\beta$ are provided by the manufacturer. Through these variations, an offset can appear in the OTA.[13]

If the differences in the parameter $V_{th}$ between any two transistors are considered and its variance is calculated (assuming there is no covariance between the parameters of the transistors) as follows:

$$\Delta V_{th} = V_{th_i} - V_{th_j}, \tag{7}$$

$$\sigma^2_{\Delta V_{th}} = \sigma^2_{\Delta V_{th_i}} + \sigma^2_{\Delta V_{th_j}} = 2\sigma^2_{\Delta V_{th_i}}, \tag{8}$$

these variations decrease as the area of the transistors increases, since they are generally caused by lack of homogeneity in the doping of the substrate. The following model is then considered for the deviation of $V_{th}$ and $\beta$.[14]

$$\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}} \tag{9}$$

$$\frac{\sigma_\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}} \tag{10}$$

Parameters $A_{V_{th}}$ and $A_\beta$ are provided by the manufacturer. Variation of $I_{\mathrm{D}}$ is caused by differences in $V_{th}$ and $\beta$ between the transistors, and it can be approximated by a first-order small signal analysis as follows:

**TABLE 2** Potentiostat transistor sizes and transconductances

| Transistor Name (See Figure 6) | W/L (μm) | Transconductance (nS) |
|---|---|---|
| M1, M2 | 18/3 | $55.2 \times 10^3$ |
| M3, M4 | 1.8/30 | 552 |
| M5 | 51.3/3 | $123 \times 10^3$ |

$$\Delta I_D = \frac{\delta I_D}{\delta V_{th}} \Delta V_{th} + \frac{\delta I_D}{\delta \beta} \Delta \beta. \tag{11}$$

Partial derivatives can be obtained from the equation of the current by the transistor in the saturation region.[15]

$$\frac{\delta I_{\mathrm{D}}}{\delta V_{th}} = -G_{\mathrm{M}}, \tag{12}$$

$$\frac{\delta I_{\mathrm{D}}}{\delta \beta} = \frac{I_{\mathrm{D}}}{\beta}, \tag{13}$$

where $G_{\mathrm{M}}$ is the transconductance of the transistors of the differential pair. From a statistical perspective, Equation 14 shows that the variance in the generated output current is as follows:

$$\sigma^2_{I_{\mathrm{D}}} = G^2_{\mathrm{M}}.\sigma^2_{V_{th}} + I^2_{\mathrm{D}} \left(\frac{\sigma_\beta}{\beta}\right)^2. \tag{14}$$

Finally, to obtain $\sigma^2_{V_{off}}$ provided by each transistor, the OTA transfer equation was used.

$$\sigma^2_{V_{off\,i}} = \frac{\sigma^2_{I_{\mathrm{D}i}}}{G^2_{\mathrm{M}}} \tag{15}$$

The constants of the deviation model in $V_{th}$ and $\beta$, provided by the manufacturer,[16] are shown in Table 3. With the transistors' sizes chosen, the resultant offset is shown in Table 4.

To obtain the total offset voltage of the circuit, Equations 16 and 17 were used as follows:

$$\sigma^2_{\mathrm{V_{off}}}\mathrm{TOTAL} = \sigma^2_{\mathrm{V_{off_{M7-8_{OTA}}}}} + \sigma^2_{\mathrm{V_{off_{M9-10_{OTA}}}}} + \sigma^2_{\mathrm{V_{off_{M1-2_{OTA}}}}} + \sigma^2_{\mathrm{V_{off_{M3-4_{OTA}}}}}, \tag{16}$$

$$V_{off_{TOTAL}} = \sqrt{\sigma^2_{V_{off}} TOTAL}. \tag{17}$$

It should be noted that transistors copying the bias current (M5 and M6) do not provide offset, and they only change the common mode voltage.

Substituting the values in Table 4 into Equations 16 and 17 yields a $V_{off_{TOTAL}} = 2.14$ mV. Assuming a minimum output resistance of 70 kΩ, the circuit has a maximum offset current of $I_{off_{TOTAL}} = \frac{2.14\ \mathrm{mV}}{70\ \mathrm{k\Omega}} = 30.6$ nA.

**TABLE 3** Deviation constants of the transistors used

| Constant | Value |
|---|---|
| $A_{V_{th}}$, NMOS | 12.9 μV/μm |
| $A_\beta$, NMOS | 1.84% μm |
| $A_{V_{th}}$, PMOS | 13.5 μV/μm |
| $A_\beta$, PMOS | 1.61% μm |

Abbreviations: NMOS, N-type metal-oxide-semiconductor; PMOS, P-type metal-oxide-semiconductor.

**TABLE 4** Operational transconductance amplifier (OTA) transistors offset

| Transistor Name (See Figure 5) | $\sigma_{V_{th}}$ | $\sigma_\beta$ | $\sigma^2_{I_D}$ | $\sigma^2_{V_{off}}$ |
|---|---|---|---|---|
| M1, M2 | 330 μ | 108 n | $7.41\ x\ 10^{-20}$ | 109 n |
| M3, M4 | 2.25 m | 24.7 n | $1.03\ x\ 10^{-18}$ | 1.52 μ |
| M7, M8, M9, M10 | 2.27 m | 27.9 n | $1.00\ x\ 10^{-18}$ | 1.48 μ |

In addition to this random offset, there is a systematic offset in the OTA that is due the circuit not being perfectly symmetrical and the fact that current mirrors are not ideal, which affects their copy ratio. Because of this effect, there will be a nonzero output current in the OTA when $V_{in+} = V_{in-}$. This effect can be corrected if the size of one of the transistors of the output current mirror is slightly modified. In our case, it was decided to decrease the length of transistor M10 by 0.2 μm (see Figure 5). This change gives a systematic offset of 0.15 mV.

## 2.2 | Current-controlled oscillator

To measure current, a circuit that is not heavily dependent on its components' actual dimensions (since manufacturing low-error resistors or capacitors in integrated circuits is expensive or impossible) was required. The circuit shown in Figure 8 was selected, and the duty cycle of the voltage signal on node *digital out* is used as an indirect current measure. A qualitative analysis of the circuit operation will follow.

In Figure 8, component U1 represents an S-R latch, components U2 and U3 represent voltage comparators, and component U4 represents a digital inverter.

If the initial conditions are that, the capacitor C1 starts from an unloaded state ($V_{[C1]} = 0$). Since voltage in the capacitor is lower than one-fourth $V_{DD}$, comparator U3 returns a high voltage output, which activates input *R* in latch U1. Therefore, output *Q* gives low voltage, which enables conduction through transistor M6. Since the comparator inputs are high impedance, and transistor M1 is cutoff, current through node *I measure* is applied directly to charge capacitor C1 (40 pF, poly-poly capacitor). Once the voltage in C1 reaches one-fourth $V_{DD}$, comparator U3 deactivates its output, but latch U1 sustains conduction through M6. Once voltage in C1 reaches three-fourth of $V_{DD}$, comparator U2 activates and thus activates the *S* input in latch U1. Therefore, output *Q* gives high voltage and enables conduction through the cascode current mirror represented by M2 to M5. Capacitor C1 discharges at a speed set by a known current $I_{ref}$. Voltage in C1 decreases until reaching one-fourth $V_{DD}$, when the entire process is restarted. This behavior is illustrated in Figure 13.

The duty cycle of the output signal is a function of the current that is not dependent on the dimensions of any component in the circuit, just on a reference current (which is known and constant) as is shown in Equation 18. This characteristic is especially useful, because it makes the measure robusts against manufacturing variations, avoiding the need for any kind of external calibration.

$$DC = \frac{\frac{V_{DD}C_1}{2I_{ref}}}{\frac{V_{DD}C_1}{2}\left(\frac{1}{I_{mes}} + \frac{1}{I_{ref}}\right)} = \frac{\frac{1}{I_{ref}}}{\frac{I_{ref} + I_{mes}}{I_{mes}I_{ref}}} = \frac{I_{mes}}{I_{ref} + I_{mes}} \tag{18}$$

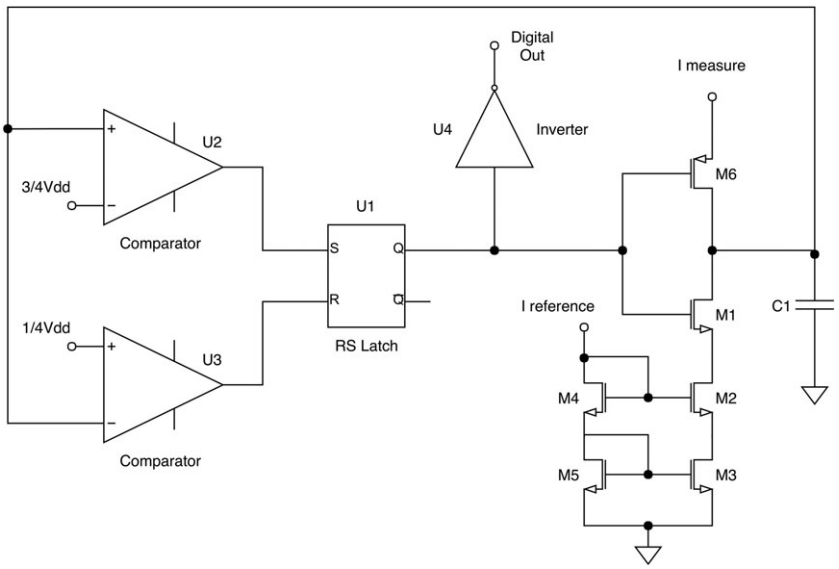


**FIGURE 8** Schematic of the current-controlled oscillator

The noise introduced by this stage is negligible when compared with that introduced by the potentiostat, which was calculated in Section 1. The comparators' (U2 and U3 in Figure 8) offset will not impact in the current measure since it will only change the period of the output signal and not its duty cycle. The reference current mirror (M2-M5 in Figure 8) will contribute noise to the measure, but its contribution is negligible when compared with that of the prior stage.

## 2.3 | Multiplexer

It was required, as part of the design specifications, that the potentiostat could operate with eight input channels. For this reason, it was necessary to include analog multiplexers connected to the auxiliary and reference electrodes of the potentiostat. For the multiplexers, the classic design was used,[17] consisting of a digital three-bit decoder controlling the activation of transmission gates. Since the design requires two multiplexers with identical activation condition, both share the same decoder.

## 2.4 | Complete circuit

Finally, all components developed in the preceding sections were joined to obtain the complete design. A schematic with the respective interconnections is shown in Figure 1. With the complete circuit, the design was validated through a simulation for different output currents within the range of 1 to 10 μA. The result is shown and discussed in Section 4, Figure 15. As seen in Figure 15, the total systematic error introduced by the circuit will be less than 0.12% of the measured current, and if the noise and offset effects are considered, even so, the total circuit error is below the 5% target.

# 3 | CIRCUIT LAYOUTS

## 3.1 | Layout techniques

Due to physical effects of the manufacturing processes, two transistors equally drawn will have not the same properties (mismatch), even if they were designed with identical dimensions. For this reason, there are several design techniques that are a more robust against the variation of the manufacturing process. The technique used in this design consists of dividing all the transistors to be paired into smaller transistors (known as "fingers") that will be intercalated and connected in series or in parallel (two transistors of dimensions [width {W}, length {L}] connected in series behave as one with dimensions [W, two L] and in parallel as one of dimensions [two W, L]).[18]

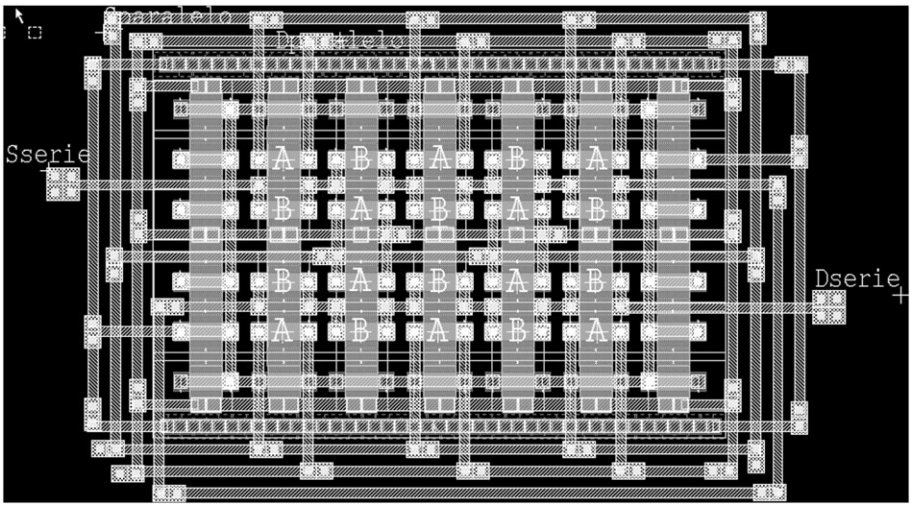


**FIGURE 9** Layout of a current mirror that was used for transistors M1 and M3 and M2 and M4 from Figure 6. Two of these instances will be needed in the potentiostat to obtain the cascode configuration

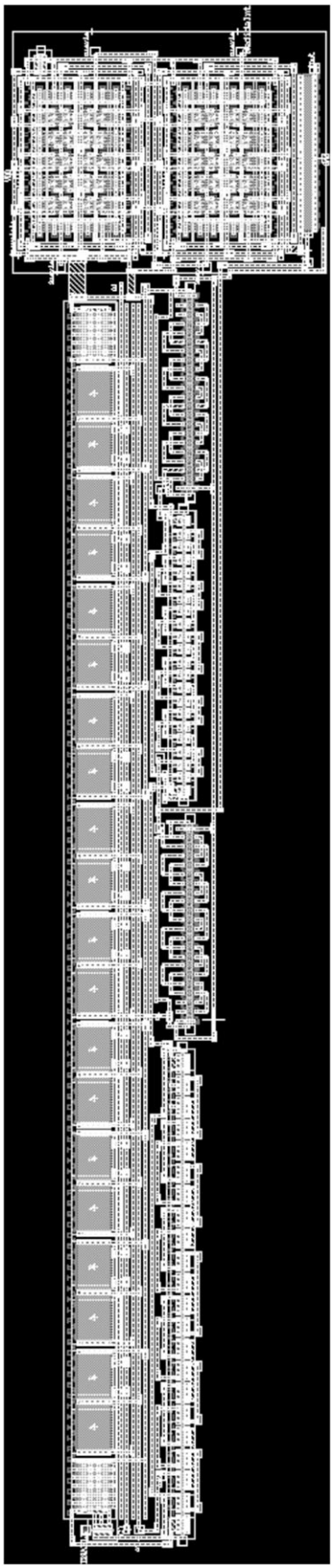

**FIGURE 10** Full layout of the potentiostat

## 3.2 | Potentiostat

The design of the potentiostat layout was approached through a modular design. The OTA and the cascode current mirrors were designed separately and instanced together, as is shown in Figures 9 and 10.

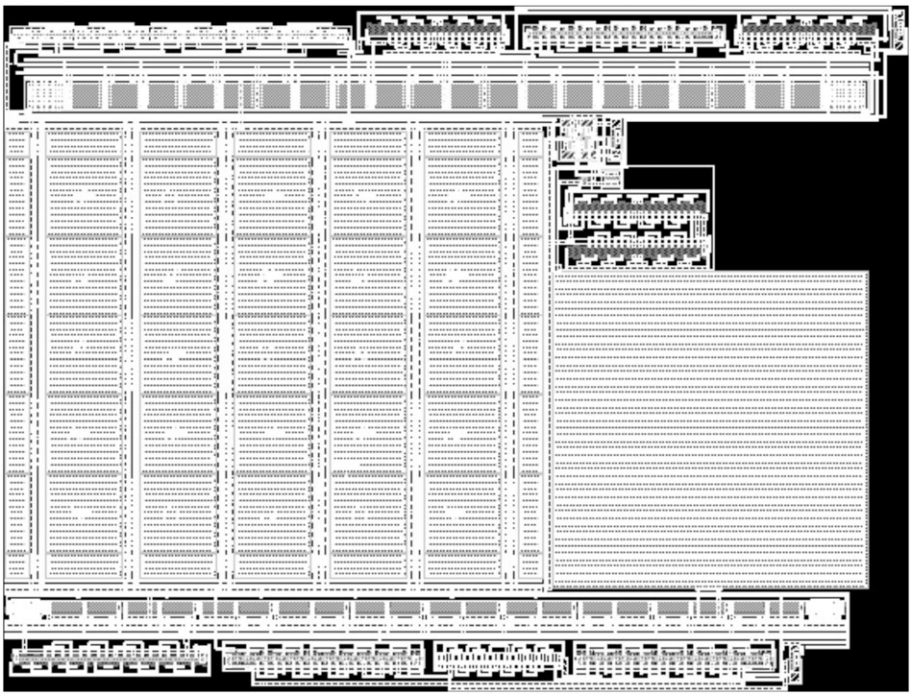

**FIGURE 11** Layout of the current-controlled oscillator

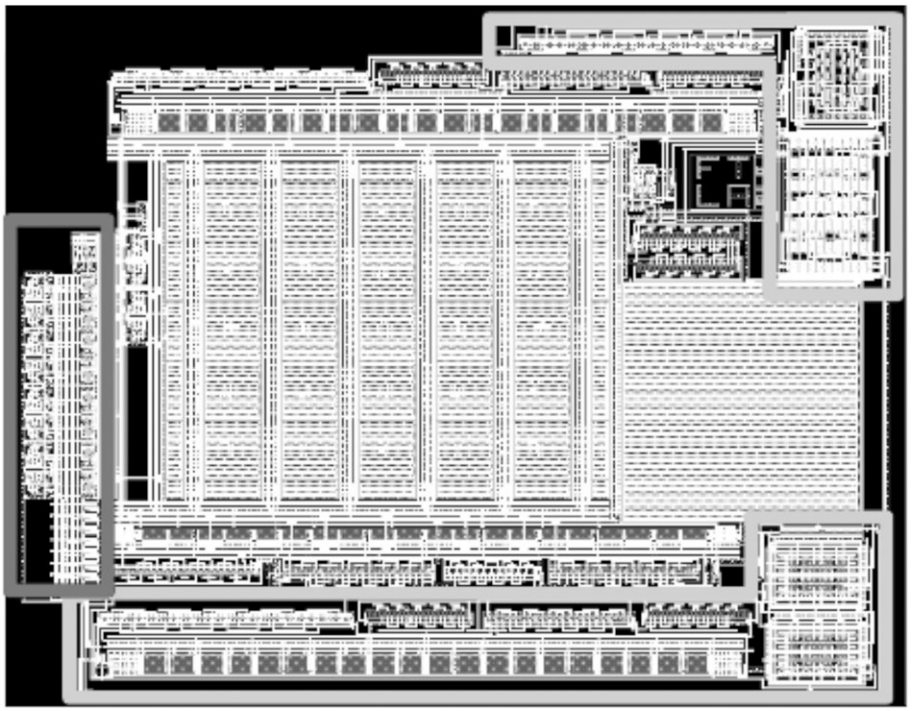

**FIGURE 12** Layout of the total circuit designed, with a total area of 0.24 $mm^2$ without pads

### 3.3 | Current-controlled oscillator

As can be seen in Figure 11, most of the area of the current-controlled oscillator is occupied by capacitors. In the center of the figure, a large capacitor matrix is used as a voltage divider for the oscillator, and on the lower right section, capacitor C1 can be seen. In the top and bottom of the figure, the comparators were placed, and above, capacitor C1 are the S-R latch and the cascode current mirror.

### 3.4 | Complete circuit

After designing all components, they were connected in a configuration to attempt to minimize silicon area, with a total area of 0.24 $mm^2$ without pads and 2.5 $mm^2$ with pads. The result can be seen in Figure 12. In the left side of the layout

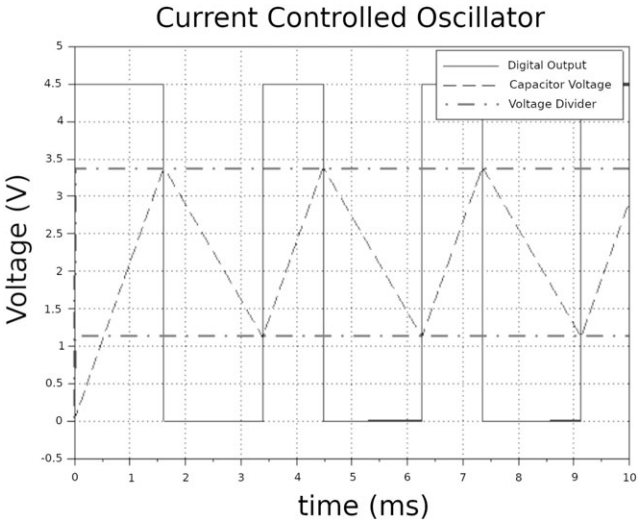


**FIGURE 13** Simulation result for the current-controlled oscillator working with an arbitrary input current

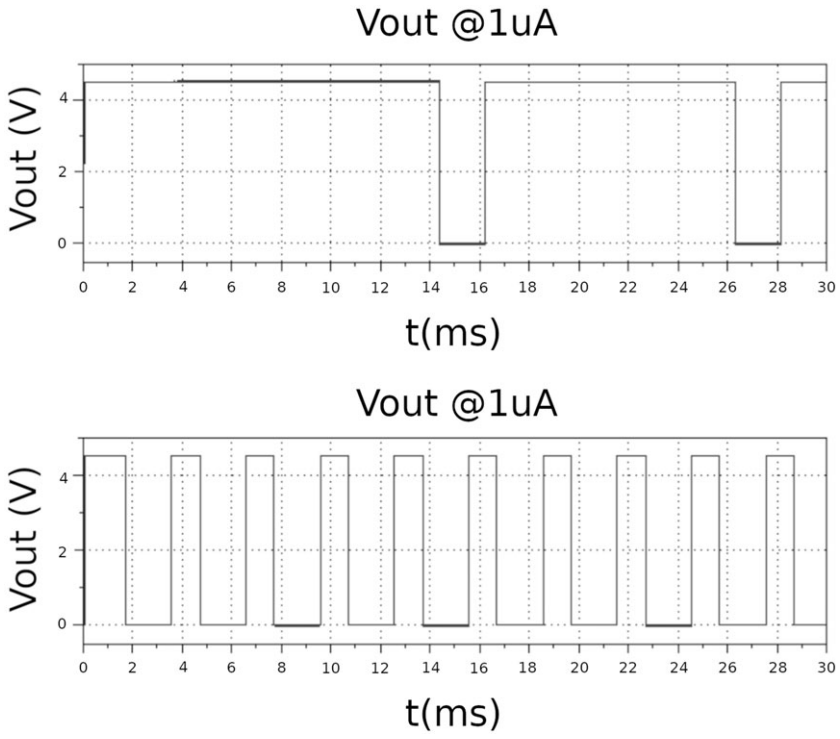


**FIGURE 14** Transient simulation of the digital output of the complete circuit with different output current

is the multiplexer, in the bottoms, the potentiostat (see Figure 10), in the center, the current-controlled oscillator (see Figure 8), and in the top right is the bias circuit.

## 4 | SIMULATION RESULTS

To validate the design, spice simulations using the BSIM3v3 model[19] were performed. First, the current-controlled oscillator was simulated with arbitrary input currents, as can be seen in Figure 13. Figure 14 depicts the output of the complete circuit when the output currents are the maximum and the minimum, respectively.

Total circuit was simulated with different values for resistances R1 and R2 (see Figure 4), which represent different blood samples. The measured current value was calculated from the output signal duty cycle, and relative error was calculated. The same process was done after adding the effects of theoretical transistor noise and statistical offset in the OTA. In all cases, the error was well under the acceptable values (below 5%). Results are shown in Figure 15.

As shown in Figure 14, the frequency and duty cycle of the output signal depend on the value of the output current of the potentiostat. The calculated values of the current from the output signal duty cycle are in this case, 0.9998 and 9.997 μA.

To see the robustness of our circuit to the manufacturing process, diverse simulations were performed. First, a corner simulation was done using the worst power and worst slow models. The results are shown in Figure 16.

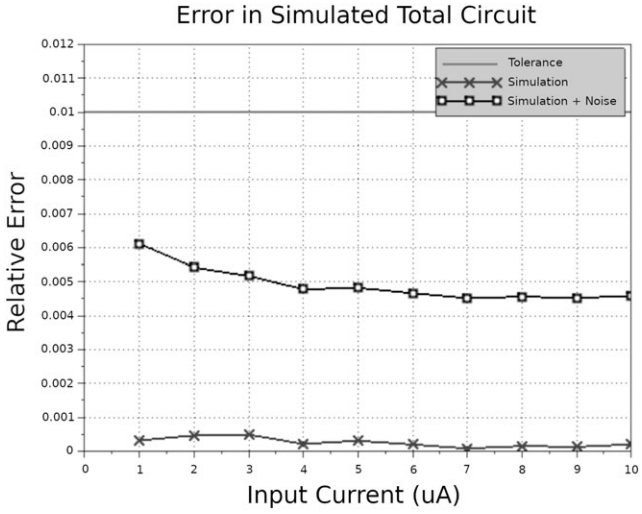


**FIGURE 15** Simulation of error in current measurement, with and without thermal and flicker noise, and statistical offset in the operational transconductance amplifier (OTA)

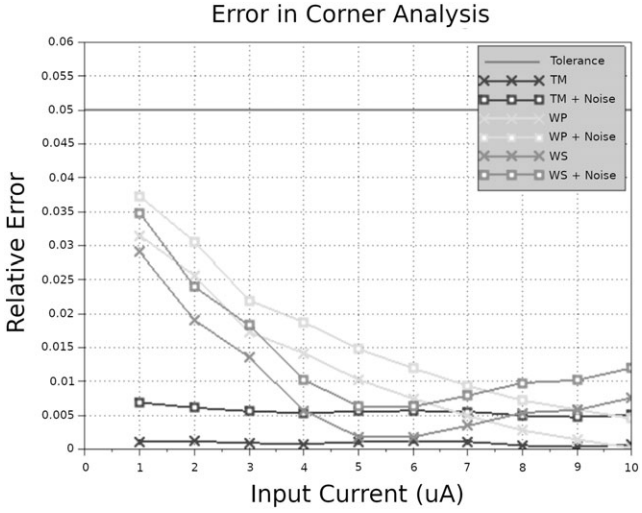


**FIGURE 16** Error and noise values for corner cases

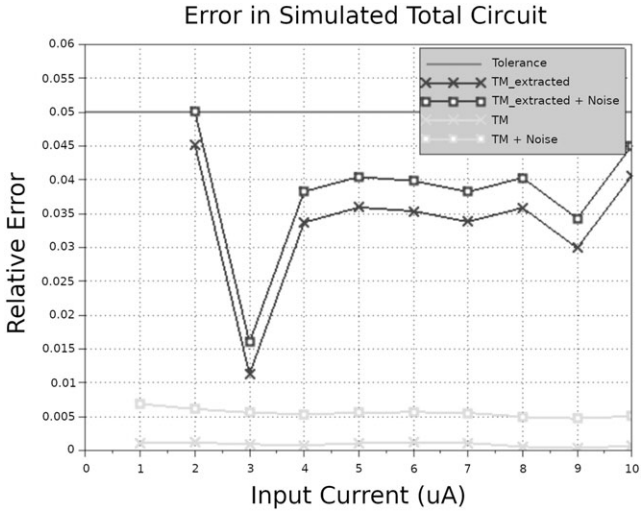


**FIGURE 17** Simulation of the error of the total circuit with layout parasitic capacitances

**TABLE 5** Target vs achieved values

| | Target | Achieved |
|---|---|---|
| Area without pads, $mm^2$ | ≤1 | 0.24 |
| Consumption, μA | ≤1 | 1.4 |
| Error, % | 1 | 0.61 |
| Supply voltage, V | <5 | 4.5 |
| Needs calibration | No | No |

As we can see, the noise is similar on all the cases but the error, as expected, is higher on the corner cases but still lower than the 5% admissible value. Finally, a layout parasitic extraction was done. The results are shown in Figure 17.

Similarly, to the corner simulation, the error is higher with the parasitic capacitances but is still lower than the allowed error for the range of interest between 1 and 10 μA.

## 5 | CONCLUSION

In this work, an integrated circuit of a potentiostat, a current-controlled oscillator, and two multiplexers were designed and simulated, aimed at the detection of the presence of Chagas disease in blood. Performance of the circuit was per expectations; Table 5 shows the target values and the values obtained in the simulation.

Although the consumption is slightly higher than the target, it was determined that the value obtained was totally acceptable, since the current efficiency of the whole circuit (measured as the ratio of the output current of the potentiostat to the total current) is between the values 40% to 87% depending on the output current. To further lower consumption, we could experiment with different copy ratios in the current mirror that scales the output current. The ASIC is to be fabricated within this year.

To properly compare our ASIC with the design, it was based on the study of Martín et al,[4] a single channel version of our circuit was designed. This reduced inputs and outputs of our circuit from 25 to eight, thus significantly reducing the area since our design is pad limited. With these modifications, a circuit with an area of 0.85 $mm^2$ was obtained, which is smaller than the 0.93 $mm^2$ reported in Martin et al.[4]

Although total current consumption is not mentioned in the study of Martin et al,[4] they mention that the bias current for the OTA of their potentiostat is 1.4 μA, since the bias current for the OTA of our ASIC is only 54 nA and the total current consumption of our ASIC is 1.4 μA lower than.[4]

Comparing with the potentiostat used in Cortina et al[5] and the one in this work provides compatible electrical specifications and all the advantages of an ASIC. This method for detection of Chagas disease has shown similar accuracy to traditional methods, as is reported in Rocha-Gaso et al and Cortina et al.[3,5]

Other applications for integrated potentiostats have been reported,[20,21] which fall within the specifications of our potentiostat. In the future, further research could be done to study its potential for detection of other diseases.

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